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Computer design of silicon Ka-band SDR impatt diode and a study on the effect of package parameters on the high frequency admittance characteristics

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Abstract Computer design of a silicon single drift region (SDR, $p^+ n n^+$ type) IMPATT diode for Ka-band operation around 35 GHz window frequency is reported in this paper D C and high frequency small signal analyses are carried out for the design of the diode Also, the effect of parasitic series resistance on the high frequency admittance characteristics of the SDR diode, embedded in a suitable device package, is studied and the results are reported

It is found that the parasitic resistance and package parameters change the admittance characteristics (G-B plots) of the diode. Increase in series resistance generally lowers the negative conductance (G) The package inductance tends to decrease the diode negative conductance, while the package capacitance increases the susceptance (B) of the device The frequence for peak negative conductance (f_p) of the diode is also found to shift downward due to presence of package parameters

Keywords Silicon Ka-band, IMPATT device, series resistance, numerical simulation

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1. Introduction

IMPATT devices have emerged as the most powerful solid state devices for generation of high power in millimetre wave frequencies, and are being widely used in mm-wave radars and guided missiles. A recent article on transit time devices by Roy provides a review of the physics and technology of IMPATT devices and systems [1]. Since the last decade, several workers have been exploring the possibility of high power generation (both CW and pulsed) at Ku and Ka bands, either from a single IMPATT diode, or from several diodes by using the power combining technique [2,3]. Power enhancement by combiner technique is difficult to achieve, since this method involves complexities in proper matching of device and circuit impedences. It has now become evident that for better understanding of the device-circuit interaction, the encapsulated device impedence and the waveguide circuit impedence should be studied separately.

In this paper, the authors present the results of d.c. and small signal computer studies on the design of flat profile SDR IMPATT diode for operation at Ka-band around 35-GHz window frequency For diode design, epilayer resistivity has been taken as 0.5 ohm-cm. The junction temperature has been set at 225°C, while the d.c. current density has been taken as 1×10^8 A/m^2. Realistic field and temperature dependence of electron and hole ionization rates and the drift velocities at 225°C have been taken [4–6], and the effect of mobile space charge has also been considered in the present computer analysis. The d.c. method, described elsewhere [7], simulates a one-dimensional model of the reverse biased p-n junction. In this method, the computation starts from the field maximum near the metallurgical junction. The dustribution of d.c. electric field and carrier currents in the depletion layer are obtained by the double iterative computer method, which involves iteration over the magnitude of field maximum (Em) and its location in the depletion layer. The method is used for a simultaneous solution of Poisson and carrier continuity equations.

The small signal analysis of an IMPATT diode provides the values of high frequency diode impedence (Z),

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conductance (G), susceptance (B), quality factor (Q), and also exhibits the range of frequencies where the diode operates with negative conductance. The small signal parameters for the present study have been obtained from Gummel-Blue method [8] with appropriate boundary conditions derived [9]. The output data obtained from the d.c. analysis have been fed as input data to the small signal equations. The effects of diode package parameters (package inductance and capacitance) on the SDR diode have also been studied, since in actual packaged diodes, the package parameters play vital roles in determining the admittance characteristics of the diode [10]. Further, the effect of parasitic series resistance has also been studied. Alderstein *et al*, developed a method for determining the series resistance from the threshold condition of IMPATT oscillation [11]. Several workers followed this approach and measured the values of series resistance of IMPATT devices operating around W-band [12] and X-band [13] frequencies. However, Alderstein's approach involves several assumptions like equal ionization rates and equal drift velocities of charge carriers. The method also incorporates an idea of average value of field derivative of ionization rates In the present method, on the other hand, the authors have obtained the device G-B plots directly from the computer based small signal analysis and accurate values of ionization rates and drift velocities of charge carriers have been obtained through computer analysis. The authors have thus studied the high frequency performance of Ka-band packaged IMPATT diode for various values of series resistance.

2. Results and discussion

Firstly, the authors have designed a silicon SDR diode for operation at Ka-band around 35 GHz frequency. The current density for SDR diode has been taken as 1×10^8 A/m^2. The diode area for SDR diode has been taken as 3×10^{-9} m^2 The breakdown voltage for SDR diode has been found to be 39 volts from computer simulation. Figures 1 to 3 show the E(x), P(x), and the doping profiles of SDR IMPATT diode. Figure 4 shows G-B plot of the designed SDR diode chip with epilayer resistivity of 0.5 ohm-cm. It is found that the peak negative conductance of the diode appears at 37.5 GHz frequency, which is very close to the desired window frequency of 35 GHz.

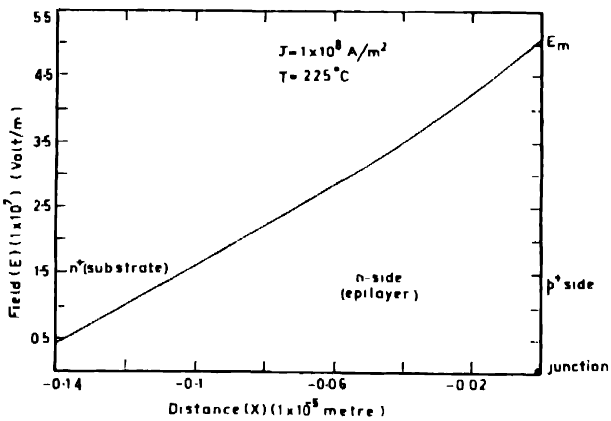


Figure 1. Field profile of silicon Ka-band SDR IMPATT diode.

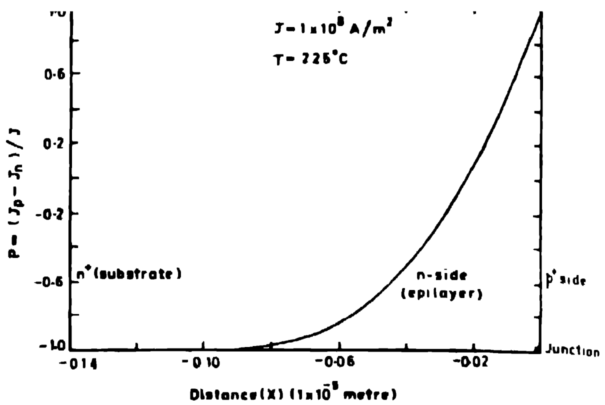


Figure 2. Normalized current density (P) profile of silicon Ka-band SDR IMPATT diode

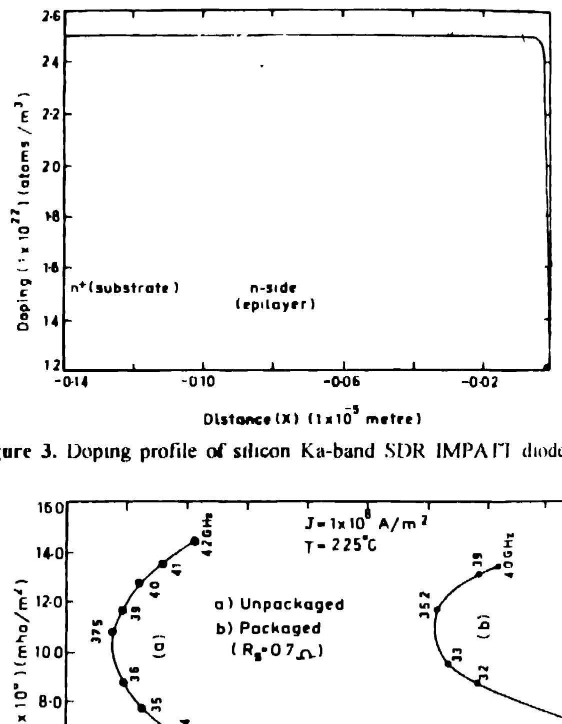


Figure 3. Doping profile of silicon Ka-band SDR IMPATT diode

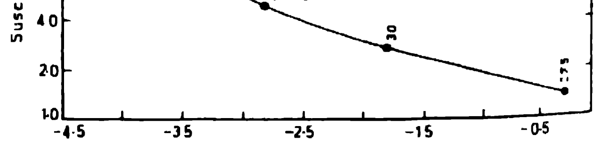
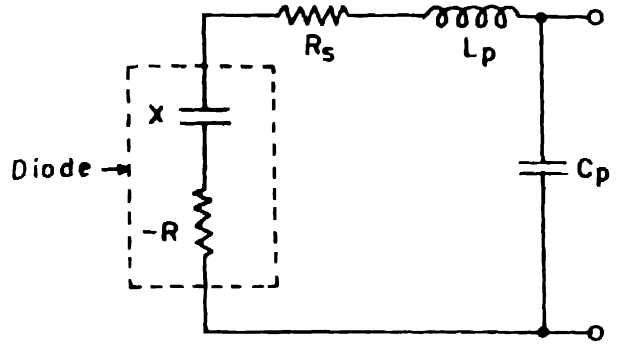


Figure 4. G-B plots of silicon Ka-band SDR IMPATT diode (unpackaged and packaged diodes)

The authors have next considered the designed SDR diode to be embedded in a package and have studied the effects of package parameters and series resistance on the high frequency admittance characteristics of the SDR diode.

The equivalent circuit diagram of a packaged IMPATT diode incorporating series resistance is shown in Figure 5.



R – Diode negative resistance
X – Diode capacitance
R_s – Series resistance
L_p = Package inductance
C_p – Package capacitance

Figure 5. Equivalent circuit diagram of a packaged IMPATT diode

Here, R_s is the series resistance, L_p and C_p are the package inductance and capacitance, respectively. The values of L_p and C_p for Ka-band packages have been taken as 0.08 nH and 0.11 pF, based on the values of package parameters supplied by the diode manufacturer [14].

Figure 4 also shows the small signal G-B plot of the packaged SDR diode with series resistance of 0.7 ohm. In this case, the diode negative conductance (G) decreases appreciably, while the diode susceptanc (B) increases due to the package capacitance, making the diode quality factor high

3. Conclusions

The authors have dsigned a SDR IMPATT diode for operation around 35 GHz frequency and have also analysed the high frequency properties of the packaged diode. The results obtained from these studies may be used for investigating the device-circuit interaction in a situation when the encapsulated diode is put in a waveguide mount for study of the oscillator characteristics of Ka-band IMPATT diodes.

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